Underfill for Ultra-Low Bumped (10µ) 3D Package

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ABSTRACT:

3D package has recently become very attractive because it can provide more flexibility in device design and supply chain, reduce the gap between silicon die and organic substrate, help miniaturize device and meet the demand of high speed, more memory, more function and low cost. With the advancement of 3D package, the bump height is now down from 80∝ to 10 ∝. When the bump diameter is 20-40∝ and height 10∝, the process and reliability are obvious issues. It is well known that underfill can enhance the reliability for regular flip chip, however it is very difficult for traditional flip chip underfill or board level underfill flow into 10∝ multi-layer of 3D package without process and reliability issues. A unique flip chip underfill series has been successfully developed, which not only function as traditional underfill such as flip chip but also work very well for 10 ∝ bump height 3D package application. YINCAE underfill series allow fast flow into 3D package and fast cure. After underfilling and cure, there are no voids observed in underfill. In this paper, a total of four different underfills have been studied. Compared to the other flip chip underfill, YINCAE underfill has demonstrated both excellent workability and outstanding reliability. In terms of workability and reliability, the four different flip chip underfills can be ranked in the following order from best to worst: A underfill > B underfill > C underfill > D underfill.

Keywords: 3D TSV package; flip chip; underfill

INTRODUCTION:

Recently 3D package has been increasingly implemented in the industry due to the flexibility in device design and supply chain, reduce the gap between silicon die and organic substrate, and the demands of size miniaturization, cost reduction, high speed and high memory, and multiple functions from end customers. In order to achieve further size miniaturization, higher speed and cost reduction, 3D TSV (Through Silicon Via) package has been introduced into the packaging industry. In addition, the bump size has been reduced from 80 ∝ to 10 ∝. However, there are some obvious process and reliability issues observed. We will discuss the process solution in our paper, "Assembly Solution to Ultra-Low Bumped 3D Package – Solder Joint Encapsulant." In order to resolve the reliability issue, underfill is being evaluated for enhancing 3D TSV package. Traditional underfill such as flip chip underfill and mold underfill have been found to have difficulty in flow into the less than 10 ∝ gap without generating void. YINCAE Advanced Material, LLC has successfully

developed unique underfill SMT 158 series by implementing special process and chemistry. In this paper we will discuss the process and reliability of 3D TSV package using the underfills from different vendors.

EXPERIMENTAL:

a. Materials:

Four underfill materials have been used in this study. A underfill (SMT 158) series are from YINCAE Advanced Materials, LLC, and three other different underfill materials from leading underfill suppliers. The properties of underfill materials are listed in Table 1. Commercial flip chip flux has been used for TSV 3D package.

Table 1. Physical Properties of Underfill Materials

Underfill	A	B	C	D
Chemistry	Epoxy	Epoxy	Epoxy	Epoxy
Filler Content (%)	60	65	50	40
Filler Size (∝)	0.2-0.3	0.6	0.3	0.8
Viscosity (Pa.s)	3.5-8	45	10	15
CTE 1/2 (ppm/K)	35/138	26/90	42/125	40/135
Tg (°C)	149	85	135	128
Curing conditions	150 °C/ 15 min	150°C/ 120 min	150 °C/ 30min	165 °C/ 90 min

b. Underfill Flowability Test:

The commercial flip chip flux was transferred into a glass slide and reflow and flux residue was left onto the glass slide. A double side tape was adhered to the two edges of the glass and then covered by another fresh glass to form the sandwich structure and the middle tunnel for underfill flow test. The sandwich of glass slides was heated up to 110 °C, and underfill was dispensed onto the end of the sandwich of glass slides and automatically flew into the sandwich tunnel. The flow time was recorded for a certain distance.

c. Pressure Cooking Test:

The underfilled flip chips were inspected via C-SAM to check underfill voids or delamination before and after pressure-cooking for seven days at 121 °C and 15 psi.

d. Thermal Cycling Test

Thermal cycling test was conducted for the underfilled flip chips. The test conditions were: -65 °C to 150 °C; 15 min each at two extreme points; 15 min for temperature ramping up from –65 °C to 150 °C and 15 min for temperature cooling down from 150 °C to –65 °C with total time of one hour per cycle.

e. Test Vehicle

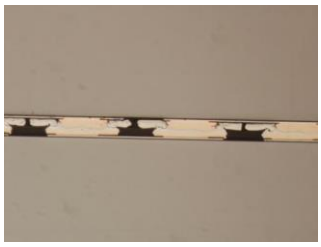

Fig.1 Part of assembled 3D TSV package

3D TSV package with 10µ bumps is assembled using thermal compression bonding process, which is shown in Fig. 1. for underfill test. Die size is 6X6mm, 100µ pitch, copper column: 8µ, pre-Sn: 2 µ.

RESULTS AND DISCUSSION:

A. The Flowability of Underfill

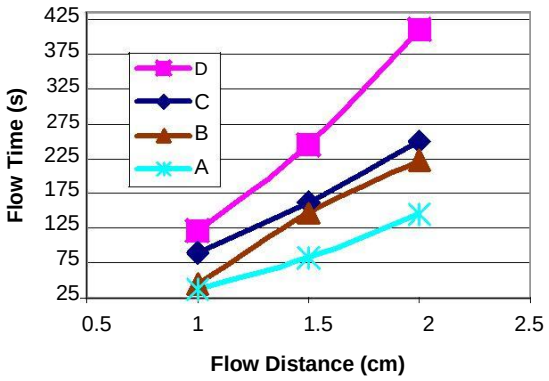

Fig. 2 Flow time vs. flow distance of underfill:

The flow test results are shown in Fig. 2. It can be seen that flow time difference is increased with the increasing flow distance. There are two factors responsible for the observation of flow time. One is that at the initial stage, the flow rate of underfill was mainly controlled by the surface tension of underfill and interaction between underfill and glass. There is some similarity among underfills from different vendors in terms of epoxy chemistry, in spite of different additives. The second is that with increasing time, the flow rate of underfill is controlled not only by the physical properties but also chemical reactions. There is different chemistry in different underfill vendor supplier. The more and quicker reactions happen at the flow time, the slower flow underfill will be. YINCAE has balanced all physical properties and chemistry very well so that A underfill has performed very well at the beginning of underfilling, much better than other competitors' underfill with increasing flow time.

B. Underfill Voids Test:

The assembled 3D TSV package has been schemed as in Fig. 3. The substrates were heated up to 110 °C and cured under the cure conditions the vendors' technical datasheet. The underfilled 3D TSV package was subject to C-SAM to check the voids. All the pictures are shown in Fig.3.

$$t = \frac{3\mu L^2}{h\gamma \cos\theta}$$

γ- Surface tension, h-separation distance, θ-wetting angle, μ-viscosity and L - flow distance

Equation 1 – underfill flow time vs. flow distance

It is very challenging for underfill to flow into 10 ∝ gaps between substrates and chips of 3D package. From the above equation, it can be clearly seen that the smaller the gap (separation distance) is, the larger specific area and capillary force have, so it is much more difficult for underfill to flow in.

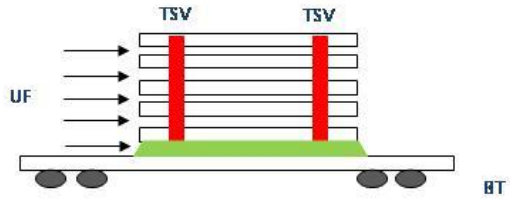

Fig. 3 Schematic 3D TSV package

Fig. 4 shows there are no voids in A underfill, but a lot of voids in other underfills. This indicates the other three underfills have difficulty in flowing in 10 ∝ gaps. It is well known that underfill voids can cause more delamination and make the reliability scarified. Due to the large percentage of underfill voids in the other three underfill, only A underfill

has passed HAST and thermal cycling reliability test.

In order to understand the reliability of flip chip underfill, regular flip chips have been used to replace 10μ bumped chip for the following pressure cooking and thermal cycling test for further comparison.

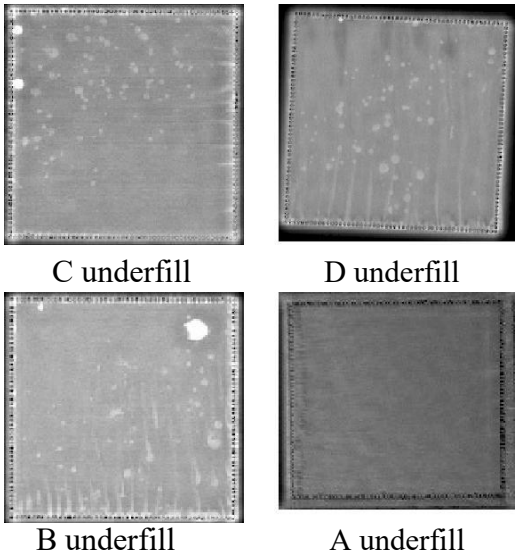

Fig. 4 C-SAM images of underfilled chips after underfill cure

C. Pressure Cook Test

In order to see the underfill difference, regular flip chips were used to replace 3D package in the pressure cooking test since before pressure cooking, the other three underfilled chips had a lot of underfill voids in 3D package. The underfilled flip chips were subject to C-SAM to check underfill delamiantion after 168 hrs pressure-cooking. Before pressure-cooking all underfills seemed acceptable. However, after pressure-cooking the underfills' behaviors were seen to be completely different. All C-SAM results after pressure-cooking 168 hrs are shown in Fig. 5.

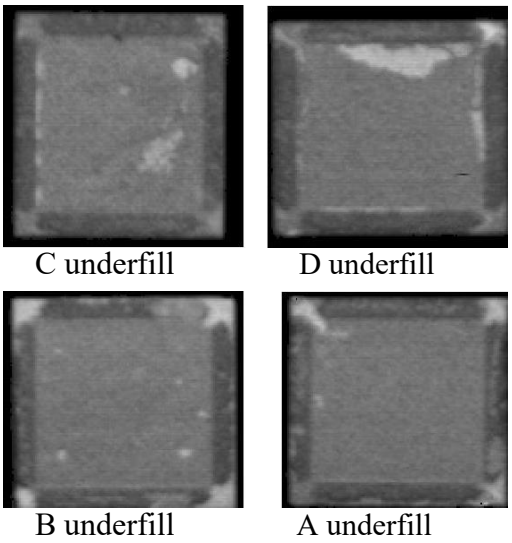

Fig. 5 C-SAM images of underfilled flip chips after 168 h pressure-cooking

It could be seen from Fig. 5 that after pressure-cooking the underfill was delaminated in the following order: D underfill > C underfill > B underfill > A underfill. There is no delamination in A underfill after 168 hrs pressure-cooking. All underfills have demonstrated different moisture resistance, which are from strong to weak in the following order: A underfill > B underfill > C underfill > D underfill. D underfill has demonstrated the weakest moisture resistance.

D. Thermal cycling Test

The underfilled flip chips were subject to C-SAM inspection after thermal cycling 1000 cycles. All C-SAM images are listed in Fig. 6.

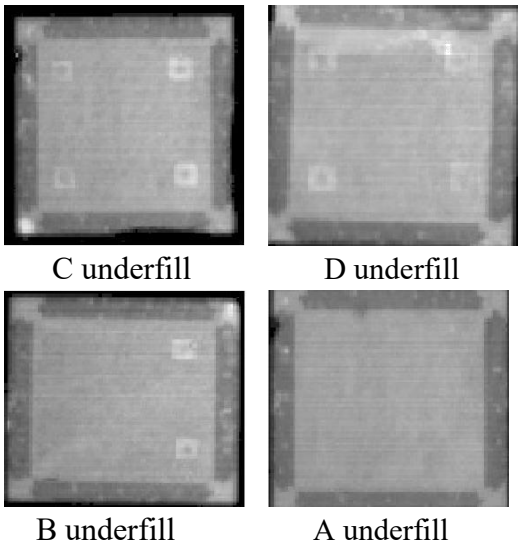

Fig. 6 C-SAM images of underfilled flip chips after 1000 hrs cycles

It could be found that C-SAM images are different from the images, which were obtained after pressure-cooking and have significant differences. However, it could still be seen that thermal resistance or thermal stability of underfills may follow the following order: A underfill > B underfill > C underfill ≅ D underfill.

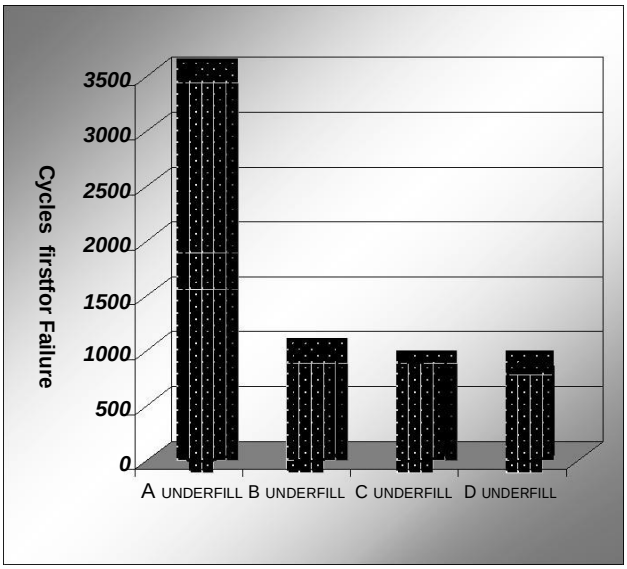

Fig. 7 The thermal cycles for first failure of underfilled flip chips.

The thermal cycles for the first electrical failure has been used for evaluation for reliability of underfilled flip chip. All the reliability data has been shown in Fig.7.

The first failure was observed for D underfill at 800 cycles, C underfill at 900 cycles, B underfill at 1000 cycles and A underfill (SMT 158) at 3500 cycles. Therefore, the reliabilities of thermal cycling are: A underfill > B underfill > C underfill > D underfill. In fact, the reliability of underfilled flip chip is the combination of underfill adhesion, moisture resistance, coefficient of thermal expansion (CTE), glass transition temperature (Tg) and thermal stability of underfill.

Of course, the reliability of underfill is strongly dependent on the underfill process. Underfill voids are usually generated in underfilling process. Underfill surface tension and flowability are the major factors of underfill voids. It is well known that underfill voids are root causes of delamination, stress accumulated center and largest CTE mismatch of micro-area. In other words, underfill voids can weaken the reliability of flip chips.

CONCLUSION:

With the advancement of 3D TSV package, it has been found that there is few underfill which can be used for 10 ∝ gap 3D TSV package. YINCAE underfill has been proved to work for 10∝ bumped 3D package. Compared with other underfills, A underfill has not only demonstrated excellent flowability and void free after underfilling, but also has passed all reliability tests for 10∝ bumped 3D package. In addition,

for underfill on regular flip chip application, A underfill has performed best both in workability and reliability. In terms of workability and reliability, flip chip underfill can be ranked in the following order from best to worst: A underfill > B underfill > C underfill > D underfill.

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